LISTING OF THE CLAIMS:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1   1: (Previously Presented) An apparatus which comprises:

2   a multi-core processor and

3   at least one test control mechanism, including at least one test access port controller

4   (TAPC) and a plurality of distributed data and control registers;

5   said multi-core processor and said test control mechanism having a configuration so as to

6   allow testing of said multi-core processor.

1   2: (original) The apparatus of claim 1, wherein said multi-core processor comprises at least two

2   processor cores and at least one circuit comprising non-processor core logic.

1   3: (original) The apparatus of claim 2, wherein said multi-core processor and said test control

2   mechanism having a configuration so as to allow testing of at least two processor cores of said

3   multi-core processor.

1   4: (Previously Presented) The apparatus of claim 2, wherein said plurality of distributed data and

2   control registers are located both within said at least two processor cores and within said at least

3   one circuit comprising non-core logic.

1   5: (original) The apparatus of claim 4, wherein said at least one test control mechanism is

2   substantially compliant with the IEEE 1149.1 specification.

1   6: (original) The apparatus of claim 4, wherein said at least one test access port controller

2   (TAPC) is located within said at least two processor cores.

1   7: (original) The apparatus of claim 4, wherein said at least one test access port controller

2   (TAPC) and at least one of said plurality of distributed data and control registers are coupled via

3   an Integrated Test Bus (ITB).

1   8: (original) The apparatus of claim 4, wherein said distributed test control mechanism is

2   controllable, at least in part, by one of said at least one test access port controller (TAPC).

1   9: (Previously Presented) The apparatus of claim 8, wherein which one of said at least one test

2   access port controllers (TAPCs) controls said distributed test control mechanism is dynamically

3   selectable during operation.

1   10: (original) The apparatus of claim 2, wherein at least one of the said at least two processor

2   cores comprises one test access port (TAP) which includes one test access port controller

3   (TAPC), and a plurality of distributed data and control registers.

1   11: (original) The apparatus of claim 10, wherein said test control mechanism and said at least

2   two processor cores are coupled so as to provide multiple coupling arrangements, said multiple

3   coupling arrangements being dynamically selectable during operation.

1   12: (original) The apparatus of claim 11, wherein said multiple coupling arrangements are

2   selected from a group consisting essentially of coupling said test access ports substantially in

3   series, coupling said test access ports substantially in parallel and coupling said test access ports

4   for substantially independent operation.

1   13: (original) The apparatus of claim 10, wherein said at least one test control mechanism is

2   arranged to allow at least one of said at least two processor cores' said one test access port (TAP)

3   to be externally visible from said multi-core processor.

1   14: (original) The apparatus of claim 13, wherein said at least one test control mechanism is

2   arranged to allow only one of said at least two processor cores' said one test access port (TAP) to

3   be externally visible from said multi-core processor.

1   15: (original) The apparatus of claim 13, wherein said at least one test control mechanism is

2   arranged to allow the selection of which at least one of said at least two processor cores' said one

3   test access port (TAP) is externally visible from said multi-core processor to occur dynamically.

1   16: (original) The apparatus of claim 10, wherein said at least one test control mechanism is

2   coupled to produce during operation an error signal if the output signals of said at least two

3   processor cores' said one test access port (TAP) are not substantially equivalent.

1   17: (original) The apparatus of claim 2, wherein said at least one test control mechanism, said at

2   least one processor core and said at least one circuit comprising non-processor core logic are

3   further coupled so as to allow testing of said at least one circuit comprising non-processor core

4   logic.

1   18: (Previously Presented) A system which comprises:

2   a computing platform, including:

3   a memory to store instructions;

4   a multi-core processor to process instructions which includes:

5   a plurality of processor cores;

6   at least one circuit comprising non-processor core logic and

7   a test control mechanism, including at least one test access port controller

8   (TAPC) and a plurality of distributed data and control registers;

9   said multi-core processor and said test control mechanism having a configuration so as to

10   allow testing of said plurality of processor cores.

1   19: (Previously Presented) The system of claim 18, wherein said multi-core processor and said

2   test control mechanism are capable of allowing testing of said at least one circuit comprising

3   non-processor core logic.

1   20: (Previously Presented) The system of claim 18, wherein said plurality of distributed data and

2   control registers are located both within said plurality of processor cores and within said at least

3   one circuit comprising non-core logic.

1   21: (original) The system of claim 20, wherein said at least one test control mechanism is

2   substantially compliant with the IEEE 1149.1 specification.

1   22: (original) The system of claim 20, wherein said at least one test access port controller

2   (TAPC) is located within said plurality of two processor cores.

1   23: (original) The system of claim 20, wherein said at least one test access port controller

2   (TAPC) and at least one of said a plurality of distributed data and control registers are coupled

3   via an Integrated Test Bus (ITB).

1   24: (original) The system of claim 20, wherein said distributed test control mechanism is

2   controlled, at least in part, by one of said at least one test access port controller (TAPC).

1   25: (Previously Presented) The system of claim 24, wherein which one of said at least one test

2   access port controllers (TAPCs) controls said distributed test control mechanism is be

3   dynamically selected during operation.

1   26: (original) The system of claim 18, wherein each of the said at least two processor cores

2   comprises one test access port (TAP) which includes one test access port controller (TAPC), and

3   a plurality of distributed data and control registers.

1   27: (original) The system of claim 26, wherein said test control mechanism and said at least two

2   processor cores are coupled so as to provide multiple coupling arrangements, said multiple

3   coupling arrangements being dynamically selected during operation.

1   28: (original) The system of claim 27, wherein said multiple coupling configurations are

2   selected from a group consisting essentially of coupling said test access ports substantially in

3   series, coupling said test access ports substantially in parallel, and coupling said test access ports

4   for substantially independent operation.

1   29: (original) The system of claim 26, wherein said test control mechanism is coupled to

2   produce, during operation, a signal that indicates whether the output signals of said at least two

3   processor cores' said one test access port (TAP) are equivalent or substantially equivalent.

1   30: (original) A method, comprising:

2   providing an indicator to identify a desired testing option;

3   based upon said desired testing option, dynamically routing signals between a plurality

4   test access ports (TAPs);

5   wherein said plurality test access ports (TAPs) are part of a multi-core processor;

6   said multi-processor core including a plurality of processor cores.

1   31: (original) The method of claim 30, wherein the routing of said signals is selected from a

2   group consisting essentially of coupling said test access ports substantially in series, coupling

3   said test access ports substantially in parallel, and coupling said test access ports for substantially

4   independent operation.

1   32: (original) The method of claim 31, wherein providing an indicator to identify a desired

2   testing option comprises storing control information in a register.

1   33: (original) The method of claim 32, wherein storing control information in a register

2   comprises shifting said data into the register in a serial fashion.

1   34: (original) The method of claim 32, wherein storing control information in a register

2   comprises a step in compliance with the operation of test data registers as described in the IEEE

3   1149.1 specification.

1   35: (original) The method of claim 30, wherein dynamically routing signals between a plurality

2   of test access ports (TAPs) comprises dynamically routing signals between a plurality of test

3   access port controllers (TAPCs) and a plurality of distributed data and control registers.

1   36: (original) The method of claim 30, wherein dynamically routing signals between a plurality

2   of test access ports (TAPs) comprises only altering the routing of signals external to said

3   plurality of processor cores.

1   37: (original) The method of claim 30, which further comprises producing a signal that indicates

2   whether the output signals of said at least two processor cores' said one test access port (TAP)

3   are equivalent or substantially equivalent.